## EXPRESS MAIL LABEL NO. EV314044234US

DATED: 28 JANUARY 2004

**ATTORNEY DOCKET: RBUS 1310-1** 

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of Inventor:

Frederick A. Ware et al.

Group Art Unit: unknown

Examiner: unknown

Application No. \_\_\_\_\_

Filed: 28 January 2004 (herewith)

Title: Communication Channel

**Calibration for Drift Conditions** 

**CUSTOMER NO. 38342** 

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

## **INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. §1.56**

Sir:

It is requested that the information identified in this statement be considered by the Examiner and made of record in the above-identified application. This statement is not intended to represent that a search has been made or that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 C.F.R. 1.56.

Enclosed with this statement is a Form PTO-SB/08. The Examiner is requested to initial the form and return it to the undersigned in accordance with M.P.E.P. 609.

Also enclosed with this statement is a copy of each cited document as required by 37 C.F.R. 1.98. The exception to this, in accordance with the 05 August 2003 Official Gazette Notice in which the USPTO waives the requirement for submitting copies of U.S. Patent and Publications for cases filed after 30 June 2003, is that copies of U.S. Patent documents and copies of U.S. Patent publications are not being submitted.

This statement should be considered under 37 C.F.R. 1.97(b) because it is being filed within three months of the filing date of an application other than a continued prosecution application under 37 C.F.R. 1.53(d).

Fee Authorization. The Commissioner is hereby authorized to charge underpayment of any additional fees or credit any overpayment associated with this communication to Deposit Account No. 50-0869 (RBUS 1310-1). A copy of this authorization is enclosed.

Respectfully submitted,

HAYNES BEFFEL & WOLFELD LLP

Date:

26 Jan 04

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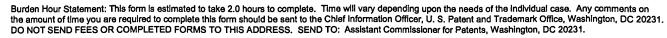
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ST	ATEMENT B	BY A	<b>NPPLICANT</b>	First Named Inventor Frederick A. Ware			
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		<del>_</del>	U.S. PATENT DOC	UMENTS	
Examiner Initials*	""" Vind Codo?		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	Al	4,384,354	Crawford et al.	05/17/1983	
	A2	5,122,978	Merrill	06/16/1992	
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	A19	2003/0026399	Carlson	02/06/2003	

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Examiner initials*	Cite No.1	Office <sup>3</sup>	Number <sup>4</sup>	Kind Code <sup>5</sup> (if known)	Applicant of Cited Document	Cited Document MM-DD-YYYY	Cited Document Pessages or Rele	Passages or Relevant Figures Appear	T <sub>6</sub>				
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	U.S. PATENT DOCUMENTS											
Examiner Initials	Cite No.1	U.S. Patent Number	Document Kind Code <sup>2</sup> (If known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear						
	A20	2001/0056		Abrosimov et al.	12/27/2001							
	A21	2002/0072	870	Adam et al.	06/13/2002							
	A22	2002/0138	224	Sessions	09/26/2002							
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Substitu	te for form 1449B/PT0	)		Complete If Known		
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INFO	DRMATION	1 D	ISCLOSURE	Filing Date	28 January 2004 (Herewith)	
STA	TEMENT	BY	APPLICANT	First Named Inventor	Frederick A. Ware	
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		OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS	
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	C1	PARIS, LLUIS ET AL, "WP 24.3 A 800MB/s 72Mb SLDRAM with Digitally-Calibrated DLL," IEEE International Solid-State Circuits Conference (1999), 13 pages.	
	C2	NAKASE, YASUNOBU ET AL, "Source-Synchronization and Timing Vernier Techniques for 1.2-GB/s SLDRAM Interface," IEEE Journal of Solid-State Circuits, Vol. 34, No. 4 (Apr. 1999), 494-501.	
	C3	GILLINGHAM, PETER, "SLDRAM Architectural and Functional Overview," SLDRAM Consortium (29 Aug 1997), 1-14.	
	C4	"Draft Standard for a High-Speed Memory Interface (SyncLink)", Draft 0.99 IEEE P1596.7-199X (1996), 56 pages	
	C5	GILLINGHAM, PETER, "SLDRAM: High-Performance, Open-Standard Memory," IEEE (1997), 29-39	
	C6	SLDRAM Inc., "400 Mb/s/pin SLDRAM," Draft Advance (9 Jul 1998), 1-69.	
	C7	ZERBE, JARED ET AL., U.S. Patent Application No. 09/776,550 filed 2 February 2001, entitled "Method and Apparatus for Evaluating and Calibrating a Signaling System."	
	C8	ZERBE, JARED ET AL, U.S. Patent Application No. 09/976,170 filed 21 October 2001, entitled "Method and Apparatus for Evaluating and Optimizing a Signaling System."	
	C9	RAMBUS "Direct Rambus Short Channel Layout Guide, Version 0.95" (August 2001), 40 pages	
	C10	RAMBUS "Direct Rambus Long Channel Design Guide" (2000), 45 pages	
	C11	RAMBUS, INC. "RDRAM Direct Rambus Clock Generator" (April 2002), 22 pages	

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	RDRAM® Overview, "High Performance Memory Interface Solution", Copyright 2003 Rar Inc., all rights reserved, 4 pages						
	C13	REDWOOD TECHNOLOGY BRIEF "High Performance Parallel Bus Interface Technology", Copyright 2003 Rambus, Inc., all rights reserved, 2 pages.					
	C14	LEWIS, DAVE, "Easy-to-Use LVDS Serdes for the Serdes Neophyte" National Semiconductor, (16 June 2003), pp. 1-5.					
	C15	INTEL "How to Measure RDRAM* System Clock Jitter" Application Note AP-667 (June 1999), pp. 1-15					
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